HCPL-2530, HCPL-2531, HCPL-4534
HCPL-0530, HCPL-0531, HCPL-0534

Dual Channel, High Speed Optocouplers

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

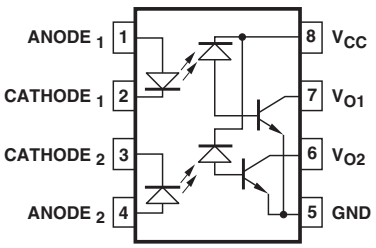
Description

These dual channel optocouplers contain a pair of light emitting diodes and integrated photo-detectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

These dual channel optocouplers are available in an 8 Pin DIP and in an industry standard SO-8 package. The following is a cross reference table listing the 8 Pin DIP part number and the electrically equivalent SO-8 part number.

8 Pin DIP	SO-8 Package
HCPL-2530	HCPL-0530
HCPL-2531	HCPL-0531
HCPL-4534	HCPL-0534

Functional Diagram



A 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

TRUTH TABLE (POSITIVE LOGIC)

LED	V_O
ON	LOW
OFF	HIGH

Features

- 15 kV/µs minimum common mode transient immunity at V_{CM} = 1500 V (HCPL-4534/0534)
- TTL compatible
- Available in 8 pin DIP, SO-8, and 8 pin DIP – gull wing surface mount (option 020) packages
- High density packaging
- 3 MHz bandwidth
- Open collector outputs
- **Safety approval**
  UL Recognized – 3750 V rms for 1 minute (5000 V rms for 1 minute for Option 020) per UL1577
  CSA Approved
  IEC/EN/DIN EN 60747-5-2
  – V_{IORM} = 630 Vpeak for HCPL-2530/2531/4534 0ption 060
  – V_{IORM} = 560 Vpeak for HCPL-0530/0531/0534 0ption 060
- Single channel version available (4502/3, 0452/3)
- MIL-PRF-38534 hermetic version available (55XX/65XX/4N55)

Applications

- Line receivers – high common mode transient immunity (>1000 V/µs) and low input-output capacitance (0.6 pF)
- High speed logic ground isolation – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL
- Replace pulse transformers – save board space and weight
- Analog signal ground isolation – integrated photon detector provides improved linearity over phototransistor type
- Polarity sensing
- Isolated analog amplifier – dual channel packaging enhances thermal tracking

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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The SO-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCPL-2530/0530 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the HCPL-2530/0530 is 7% minimum at I_F = 16 mA.

The HCPL-2531/0531 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the HCPL-2531/0531 is 19% minimum at I_F = 16 mA.

The HCPL-4534/0534 is an HCPL-2531/0531 with increased common mode transient immunity of 15,000 V/µs minimum at V_{CM} = 1500 V guaranteed.

Selection Guide

Minimum CMR			8-pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/µs)	V_{CM} (V)	Current Transfer Ratio (%)	Dual Channel Package	Single Channel Package*	Dual Channel Package	Single Channel Package*	Single Channel Package*	Single and Dual Channel Packages*
1,000	10	7	HCPL-2530	6N135	HCPL-0530	HCPL-0500	HCNW135	
		19	HCPL-2531	6N136 HCPL-4502	HCPL-0531	HCPL-0501 HCPL-0452	HCNW136 HCNW4502	
15,000	1500	19	HCPL-4534	HCPL-4503	HCPL-0534	HCPL-0453	HCNW4503	
1,000	10	9						HCPL-55XX HCPL-65XX 4N55

* Technical data for these products are on separate Avago publications.

Ordering Information

HCPL-2530, HCPL-2531, HCPL-4534, HCPL-0530, HCPL-0531 and HCPL-0534 are UL Recognized with 3750 Vrms for 1 minute per UL1577 and are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant	Non RoHS Compliant							
HCPL-2530 HCPL-2531 HCPL-4534	-000E	No option	300mil DIP-x						50 per tube
	-300E	-300		X	X				50 per tube
	-500E	-500		X	X	X			1000 per reel
	-020E	-020					X		50 per tube
	-320E	-320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
	-060E	-060						X	50 per tube
	-360E	-360		X	X			X	50 per tube
	-560E	-560		X	X	X		X	1000 per reel
HCPL-0530 HCPL-0531 HCPL-0534	-000E	No option	SO-8						100 per tube
	-500E	-500		X	X	X			1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-2530-560E to order product of 300mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

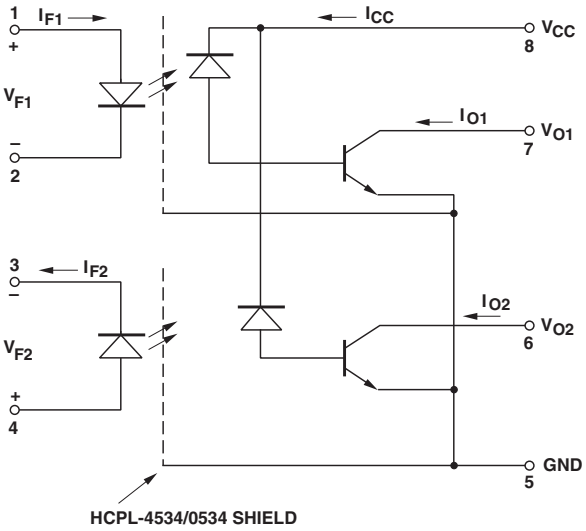
Example 2:

HCPL-2530 to order product of 300mil DIP package in tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

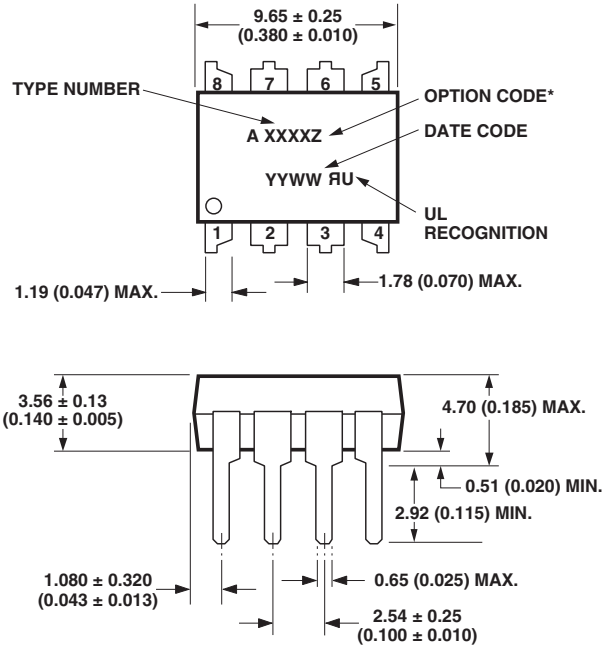
Schematic

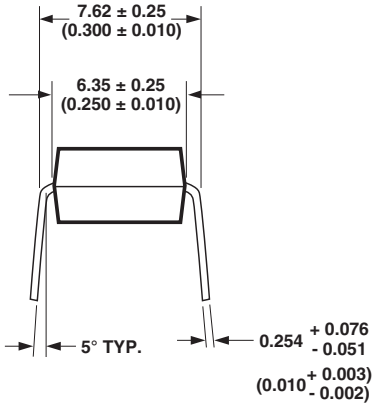


USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED.

Package Outline Drawings

8-Pin DIP Package (HCPL-2530/2531/4534)



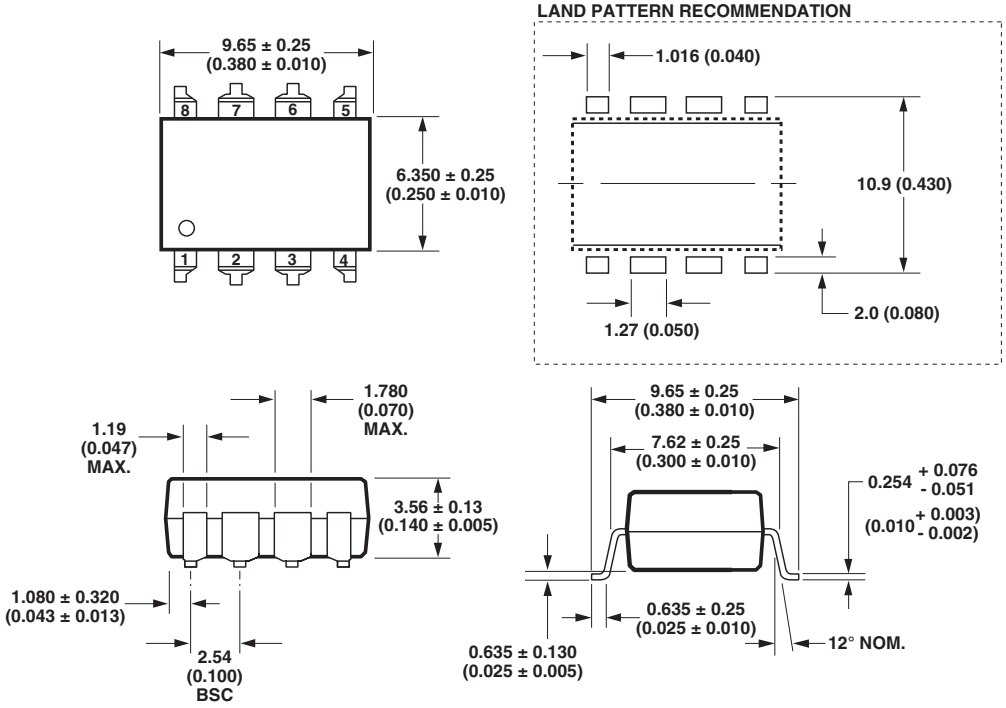


DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Package Outline Drawings, continued

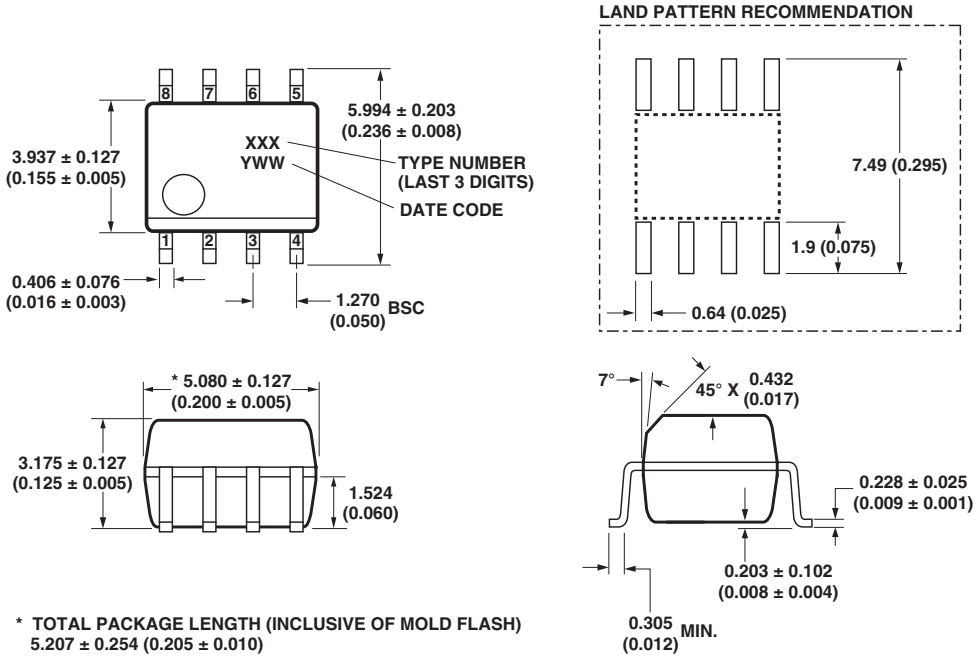
8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2530/2531/4534)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Small Outline SO-8 Package (HCPL-0530/0531/0534)

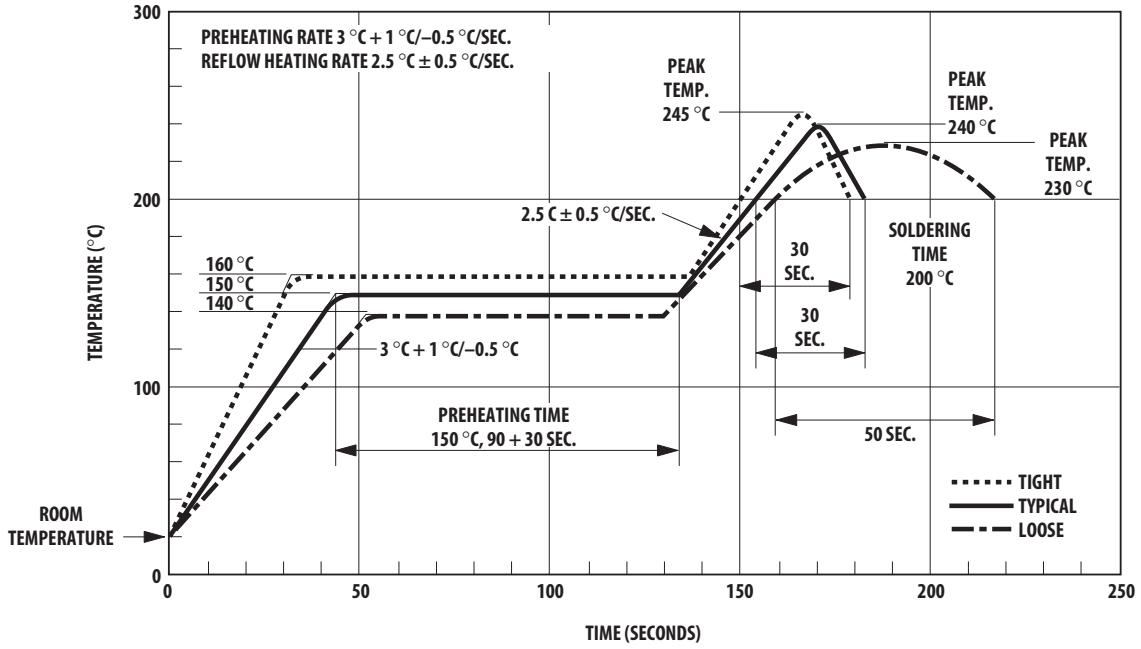


* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

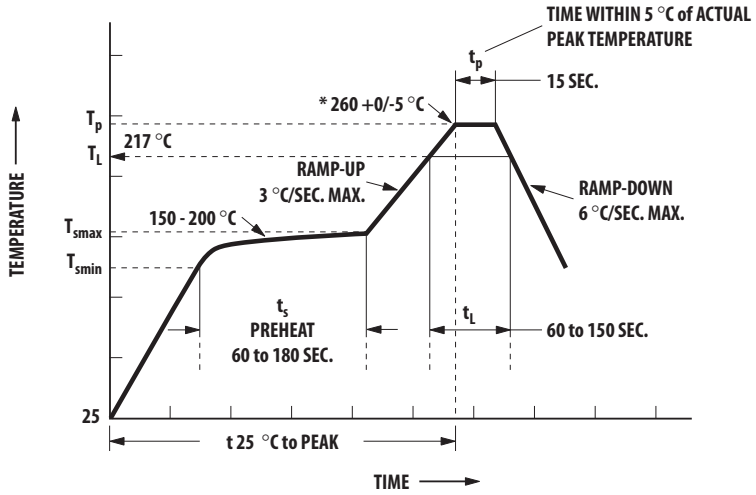
NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Solder Reflow Thermal Profile



NOTE: NON-HALIDE FLUX SHOULD BE USED.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

NOTE: NON-HALIDE FLUX SHOULD BE USED.

* RECOMMENDED PEAK TEMPERATURE FOR WIDEBODY 400mils PACKAGE IS 245 °C

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2

Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01.
(Option 060 only)

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output to to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

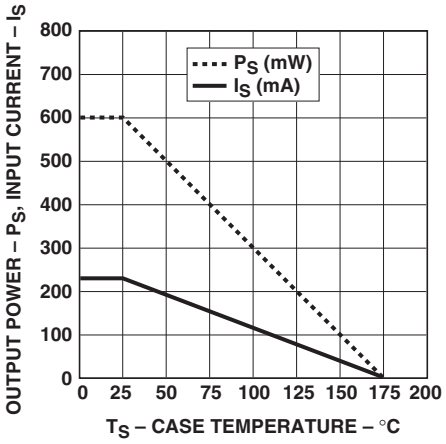
IEC/EN/DIN EN 60747-5-2 Insulation Characteristics (Option 060)

Description	Symbol	Characteristic HCPL-2530/2531/4534	HCPL-0530/0531/0534	Unit
Installation classification per DIN VDE 0110/1.89, Table 1				
for rated mains voltage ≤ 150 V rms			I-IV	
for rated mains voltage ≤ 300 V rms		I-IV	I-III	
for rated mains voltage ≤ 600 V rms		I-III	I-II	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	567	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	1050	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	840	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	4000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure.)				
Case Temperature	T_S	175	150	˚C
Input Current**	$I_{S,INPUT}$	230	230	mA
Output Power**	$P_{S,OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$> 10^9$	$> 10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-2, for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in application.



Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature	T_A		-55	100	°C	
Average Forward Input Current (each channel)	$I_{F(AVG)}$			25	mA	
Peak Forward Input Current (each channel) (50% duty cycle, 1 ms pulse width)	$I_{F(PEAK)}$			50	mA	
Peak Transient Input Current (each channel) (≤ 1 µs pulse width, 300 pps)	$I_{F(TRANS)}$			1	A	
Reverse LED Input Voltage (each channel)	V_R			5	V	
Input Power Dissipation (each channel)	P_{IN}			45	mW	
Average Output Current (each channel)	$I_{O(AVG)}$			8	mA	
Peak Output Current	$I_{O(PEAK)}$			16	mA	
Supply Voltage (Pin 8-5)	V_{CC}		-0.5	30	V	
Output Voltage (Pins 7-5, 6-5)	V_O		-0.5	20	V	
Output Power Dissipation (each channel)	P_O			35	mW	13
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds	T_{LS}	8 Pin DIP		260	°C	
Reflow Temperature Profile	T_{RP}	SO-8 and Option 300	see **Package Outline Drawings** section			

Electrical Specifications (DC)

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 9.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Current Transfer Ratio	CTR	HCPL-2530/ 0530	7	18	50	%	T_A = 25°C	I_F = 16 mA, V_{CC} = 4.5 V, V_O = 0.5 V	1, 2, 4	1, 2
			5							
		HCPL-2531/ 0531 HCPL-4534/ 0534	19	24	50	%	T_A = 25°C			
			15							
Logic Low Output Voltage	V_{OL}	HCPL-2530/ 0530		0.1	0.5	V	T_A = 25°C I_O = 1.1 mA	I_F = 16 mA, V_{CC} = 4.5 V	1	1
					0.5		I_O = 0.8 mA			
		HCPL-2531/ 0531 HCPL-4534/ 0534		0.1	0.5	V	T_A = 25°C I_O = 3.0 mA			
					0.5		I_O = 2.4 mA			
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C V_{CC} = V_O = 5.5V, I_F = 0 mA	I_F = 0 mA	6	1
					50		T_A = 25°C V_{CC} = V_O = 15V, I_F = 0 mA			
Logic Low Supply Current	I_{CCL}			100	400	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V			
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_F = 0 mA, V_O = Open, V_{CC} = 15 V			
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C I_F = 16 mA		3	1
					1.8					
Input Reverse Breakdown Voltage	BV_R		5			V	I_R=10 µA			1
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/ °C	I_F = 16 mA			
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V		1	

*All typicals at T_A = 25°C.

Switching Specifications (AC)

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	2530/0530		0.2	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	6, 7
					2.0					
		2531/0531/ 4534/0534		0.2	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time High to Logic at Output	t_{PLH}	2530/0530		1.3	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 9, 11	6, 7
					2.0					
		2531/0531/ 4534/0534		0.6	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	2530/0530	1	10		kV/µs	R_L = 4.1 kΩ	I_F = 0 mA,	10	5, 6, 7
		2531/0531	1	10			R_L = 1.9 kΩ	T_A = 25°C,		
		4534/0534	15	30			R_L = 1.9 kΩ	V_{CM} = 10 V_{p-p}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	2530/0530	1	10		kV/µs	R_L = 4.1 kΩ	I_F = 0 mA,	10	5, 6, 7
		2531/0531	1	10			R_L = 1.9 kΩ	T_A = 25°C,		
		4534/0534	15	30			R_L = 1.9 kΩ	V_{CM} = 10 V_{p-p}		
Bandwidth	BW			3		MHz	R_L = 100 kΩ		7, 8	

*All typicals at T_A = 25°C.

Package Characteristics

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		3750			V rms	RH < 50%, t = 1 min.,		3, 10
		HCPL-2530/2531 /4534 Option 020	5000						3, 11
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	RH ≤45% V_{I-O} = 500 Vdc, t = 5 s		3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz, T_A = 25°C		12
Input-Input Insulation Leakage Current	I_{I-I}			0.005		µA	RH ≤45%, t = 5 s, V_{I-I} = 500 Vdc		4
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω			4
Capacitance (Input-Input)	C_{I-I}	HCPL-2530/ 2531/4534		0.03		pF	f = 1 MHz		4
		HCPL-0530/ 0531/0534		0.25					

*All typicals at T_A = 25°C.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

Notes:

1. Each channel.
2. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
3. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
5. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
6. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
7. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and the 6.1 kΩ pull-up resistor.
8. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
9. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
11. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥6000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).
12. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
13. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C for the SOIC-8 package.

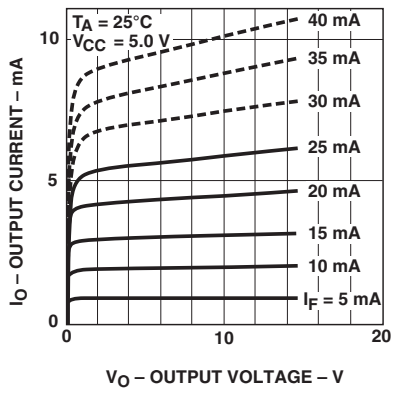


Figure 1. DC and pulsed transfer characteristics.

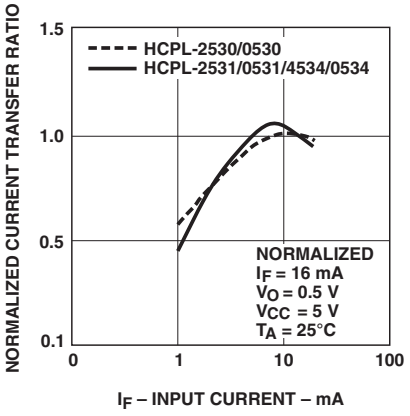


Figure 2. Current transfer ratio vs. input current.

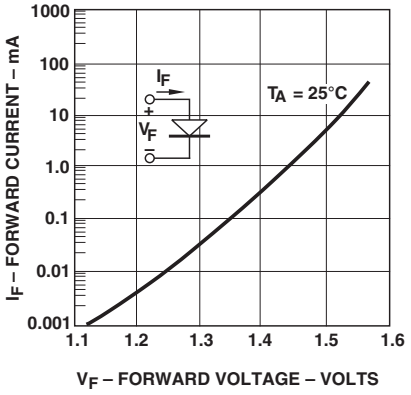


Figure 3. Input current vs. forward voltage.

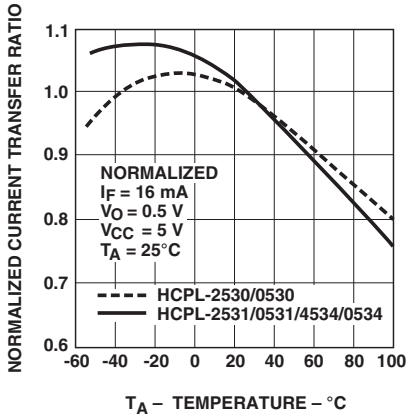


Figure 4. Current transfer ratio vs. temperature.

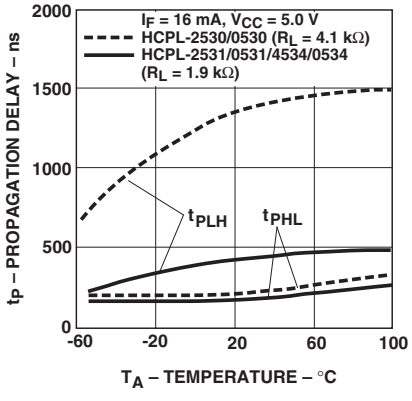


Figure 5. Propagation delay vs. temperature.

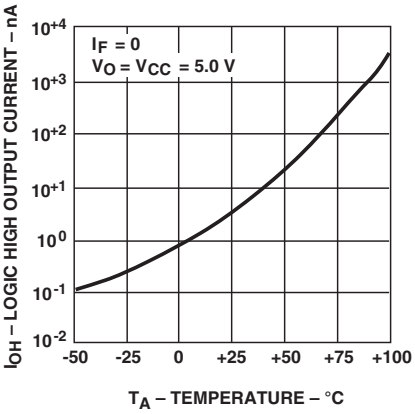


Figure 6. Logic high output current vs. temperature.

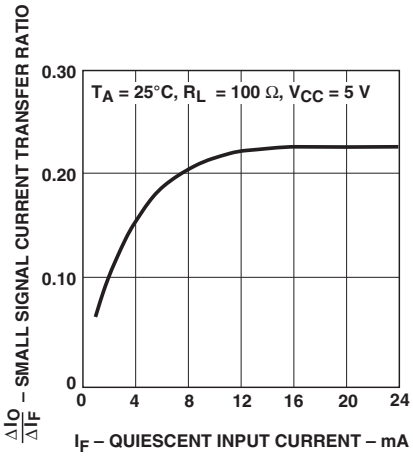
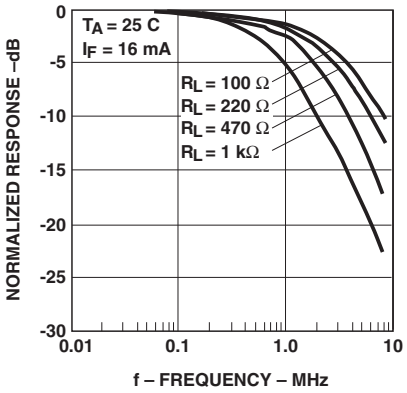


Figure 7. Small-signal current transfer ratio vs. quiescent input current.



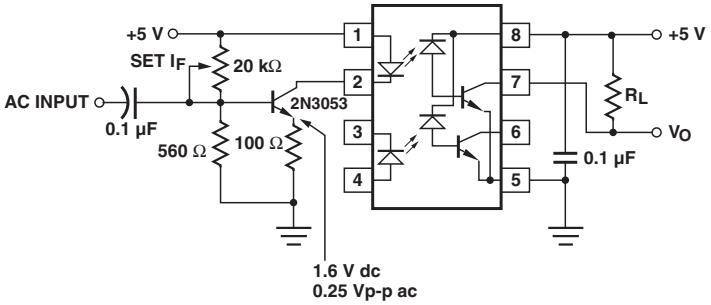
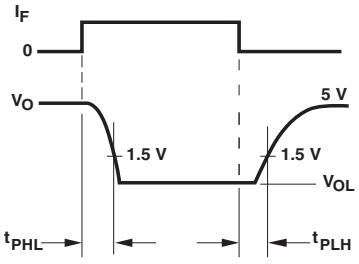


Figure 8. Frequency response.



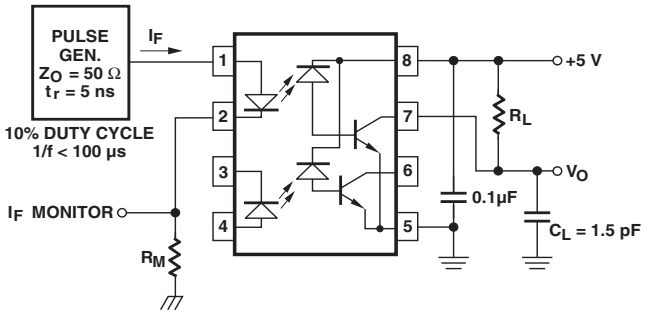


Figure 9. Switching test circuit.

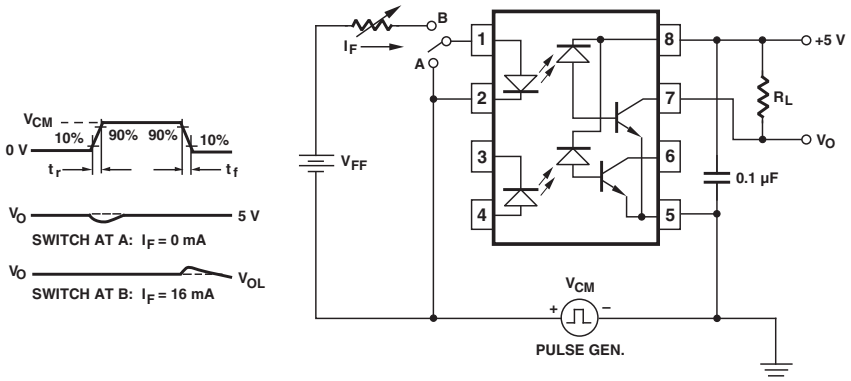


Figure 10. Test circuit for transient immunity and typical waveforms

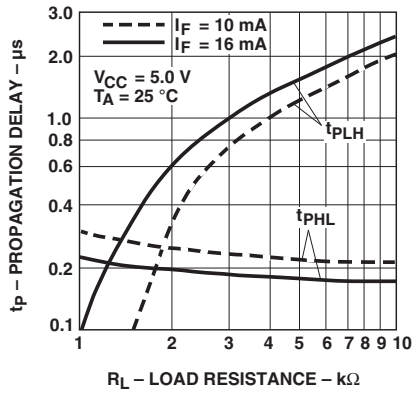


Figure 11. Propagation delay time vs. load resistance

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