DIGITAL AUDIO SOLUTIONS

archwave

Bebob Product Information

Advanced Product Information DM1500E and DM1100E/F

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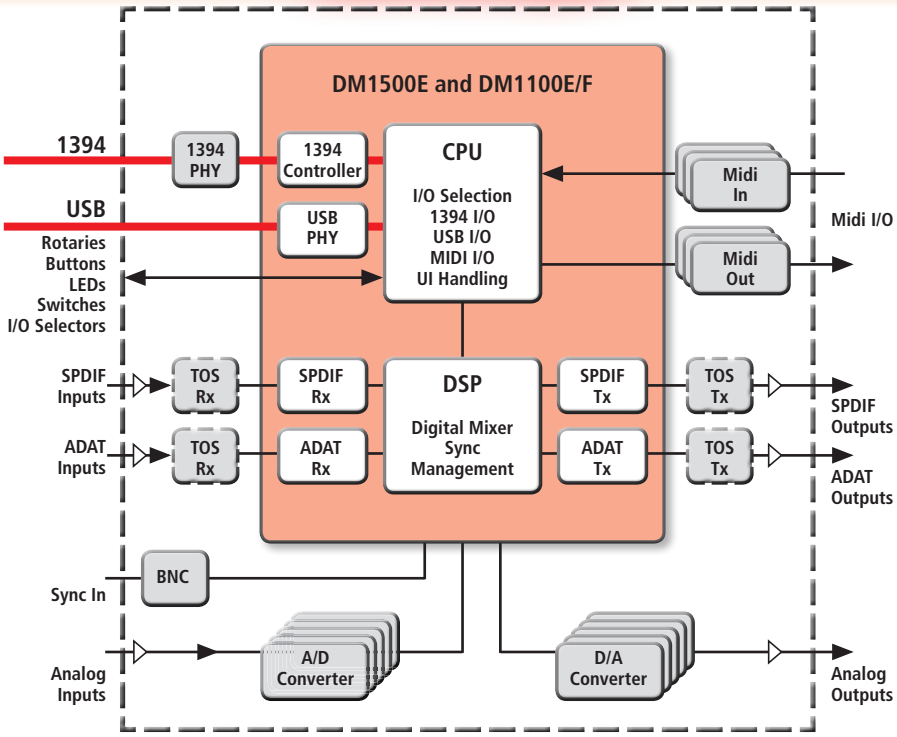
Bebob Block Diagram



Introduction

The DM1500E and DM1100E/F Media Networking Processors are highly flexible interface processors optimized for secure, real-time encoding/decoding and processing of multichannel media content. They feature an on-chip, IEEE1394 LLC, USB OTG Controller and PHY and a direct, glueless interface to PCMCIA compliant devices. The DM1500E and DM1100E/F support industry standard networking and I/O protocols and incorporate the interface and processing blocks described in Figure 1.

The DM1500E and DM1100E/F IC and the available software packages form a turnkey solution, are enabling rapid product development by OEMs and ODMs. The software packages feature an intuitive Application Programming Interface (API) that allows easy customization, resulting in fast time to market.

The DM1100E/F is fully pin- and function-compatible with the DM1500E. The DM1100E/F can support internal clock speeds up to 110 MHz, while the DM1500E offers rates up to 150 MHz. Reference designs and application software packages are available for a number of products – please consult the respective Application Product Brief for an overview of the capabilities.

Features

Secure High-performance audio/video Media Networking Processor, featuring:

- Five A/V ports offering the following interfacing capabilities when used in audio mode
- I2S: up to 32 audio channels at up to 192 kHz; master and slave mode; glueless connection to AD/DA converters
- I8S: up to 128 channels at 48 kHz / 64 channels at 96 kHz: master and slave mode; glueless connection to DSPs
- DSD: up to 16 channels at up to 12.288 MHz; input and output
- SPDIF: up to 8 interfaces (16 channels) at up to 192 kHz; input and output; integrated receiver and transmitter
- ADAT: up to 4 interfaces (32 channels) at 48 kHz; supports SMUX-II; input and output; integrated receiver and transmitter

One of the A/V ports can be used in a video mode, offering the following interfacing capabilities:

- DVB-SPI interface, 8-bit wide, 27 MHz, input or output
- MPEG-TS
- DV-SD, DV-HD, and DV-SDL
- Built-in IEEE1394a/b hybrid Link Layer Controller; supports data rates from s100 to s800: standardized interface to external 1394a or 1394b PHY
- Built-in USB 2.0 OTG Dual-Role Controller and PHY; supports HighSpeed, FullSpeed and LowSpeed; supports INT, BULK, and ISOCH transactions
- System Extension Interface to connect PCMCIA-, CompactFlash-, or ATA/ATAPI-compliant devices or other components
- Two UARTs with MIDI rate support
- SPI interface with master/slave capabilities
- ARM926EJ-S CPU at up to 150 MHz (DM1100E/F: 110 MHz): features I/D cache, I/D tightly coupled memory, and an MMU
- Real-Time Media Processor at up to 150 MHz (DM1100E/F: 110 MHz); features I cache, and I/D tightly coupled memory with direct DMA access

- High performance multichannel DMA
- SD/SRAM interface, supporting SDRAM with up to 150 MHz (DM1100E/F: 110 MHz)
- 96 kByte on-chip General Purpose SRAM
- On-chip clock multiplier, generating all internal frequencies from a single crystal
- Two on-chip audio/video PLLs for clock recovery
- Two on-chip synthesizers for clock synthesis
- Four independent clock domains
- Support for DTCP/5C encryption, decryption, and authentication for interfaces to IEEE1394 and USB
- JTAG Debug interface.

Example Applications

Consumer Electronic Products

1394 and USB networking for Pro-Audio and Consumer-Audio electronics and set-top devices.

Musical Instrument Breakout Boxes

1394 and USB digital audio recording and playback devices for flexible content creation systems.

External PC Sound Cards

PC audio output to high performance peripherals and consumer electronics devices, for a superior consumer audio experience.

Hardware Description

IEEE1394 Interface

The built-in IEEE1394a/b Link Layer Controller (LLC) supports data rates of s100, s200, s400, and s800. It connects any IEEE1394a-2000 or IEEE1394b-2002 compliant PHY to the IEEE1394a PHY, using the standard parallel interface. CAT-5 cables, Plastic Optical Fibre (POF) and Glass Optical Fibre (GOF) are supported through the use of an IEEE1394b-compliant PHY.

A dedicated clock output provides the clock to the IEEE1394a PHY, making an additional crystal unnecessary. The PHY-Link interface can be used in direct or (electrically) isolated mode. The LLC is fully isochronous-capable, as standardized by IEEE1394, and provides Cycle Master, Isochronous Resource Manager, and Bus Manager functionalities. It supports asynchronous transactions and asynchronous streams, plus isochronous streams.

An IEC61883-compliant framing/deframing and, depending on the operating system version, DTCP/5C copy protection functionality is provided through firmware. Isochronous and asynchronous data received through the IEEE1394 interface is written to the on-chip General.

Purpose SRAM, the external SD/SRAM or the RTM Processor's Tightly Coupled RAM (TCRAM), depending on configuration. Data to be transmitted is buffered in one of these locations and written to the IEEE1394 interface. These transfers are autonomously performed by DMA.

USB 2.0 Interface

The integrated USB 2.0 On-The-Go Controller (Dual-Role) supports Host and Device controller functions. In Host mode, it supports HighSpeed (480Mbps), FullSpeed (12Mbps) and LowSpeed (1.5Mbps), and offers point-to-point connectivity with one USB device. In Device mode, it supports HighSpeed (480Mbps) and FullSpeed (12Mbps). An integrated PHY offers a direct USB interface without the need for external active components. 12 endpoints are available. These Endpoints can be configured to use either INT, BULK, and ISOCH transactions. High Bandwidth endpoints are supported for INT and BULK. A total of 16 kByte RAM is available for Endpoints FIFOs, and double buffering can be enabled for any endpoint. Data received or to be transmitted is buffered in the appropriate Endpoint FIFO. Either the ARM CPU, the RTM Processor or DMA can access the Endpoint FIFOs.

Audio Interface

The DM1100F/DM1500E provides five audio/video ports. Each of these ports can be configured independently, as follows:

- Port0 and Port1 offer both an audio and a video mode. In the audio mode, Port0 supports DSD, I2S or I8S on four data interfaces. In the video mode, Port0 and Port1 are combined to offer a DVB-SPI compliant 8-bit video interface, which can carry uncompressed ITU-R BT.656 or compressed MPEG-TS or DV video.
- Port2 and Port3 both support audio as I2S, I8S, DSD and SPDIF.
- In the audio mode Port4 supports DSD, ADAT/SMUX, I2S and I8S on four data interfaces.

Audio sampling rates up to 192 kHz are supported on all ports. Audio data formats include 16-bit, 20-bit, 24-bit and 32-bit.

Data received through the audio/video ports is written to the on-chip General Purpose SRAM, the external SD/SRAM or the RTM Processor's TCRAM, depending on the specific system configuration. Data to be output on the audio/ video port is buffered on one of these locations, and is then written to the interface. These transfers are autonomously performed by the DMA block. Ordering Guide Bebob can be ordered as one of the three following components: SDK (Software Development Kit) DDK (Driver Development Kit – for Windows only) Bebob Reference Board.

Control Interfaces

The DM1100F/DM1500E features a Serial Peripheral Interface (SPI) with two dedicated chip selects. Further chip select lines can be added by using General Purpose I/O (GPIO) signals. The SPI interface is one of the two selectable boot sources, i.e. a serial FLASH can be connected to this interface. The SPI interface features high bit rates up to 37 Mbps (DM1100E/F: 25 Mbps), and supports peripherals with high throughput requirements, including displays, network interfaces, or other CPUs.

Two Universal Asynchronous Receiver/Transmitter interfaces (UARTs) are integrated, with Tx and Rx lines. The UARTs support a broad range of baud rates, including the specific MIDI rates.

All control interfaces can be accessed through either the ARM CPU or the RTM Processor.

Processors

ARM9

The ARM926EJ-S core features both DSP and Java extensions, and runs at frequencies up to 150 MHz (DM1100E/F: 110 MHz). The memory configuration includes a 4 kByte Instruction Cache, 4 kByte Data Cache, 16 kByte tightly-coupled Instruction RAM (TC RAM), and 8 kByte tightly-coupled Data RAM. A vector interrupt controller ensures the shortest possible interrupt latencies.

The ARM CPU can access and execute code from the on-chip General Purpose RAM, and from external SD/SRAM or FLASH. It can also access a number of on-chip resources, such as the USB Controller, SPI and UARTs. The ARM CPU is booted either serially (SPI) or through the parallel memory interface, depending on the chosen configuration.

Real-Time Media Processor

The RTM Processor features a data width of 32 bits, and runs at up to 150 MHz (DM1100F: 110 MHz). The memory configuration includes 4 kByte of Instruction Cache and 12 kByte of tightly coupled RAM, which can be shared between data and instructions. The TC RAM is also accessible by DMA or the ARM CPU, enabling high I/O throughput.

The RTM Processor can access and execute code from the on-chip General Purpose RAM and from external SD/SRAM or Flash. It can also access a number of on-chip resources, such as the USB Controller, SPI and UARTs.

The RTM Processor is boot-strapped by the ARM926EJ-S CPU.

Software

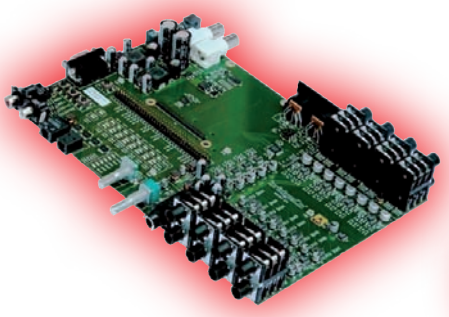
A comprehensive set of Bebob software modules and complete reference applications is available for the DM1500. The application software is based on Archwave's Kernel & OS (KnOS), an industry proven real-time multithreaded kernel, optimized for data streaming and data handling.

The KnOS API provides abstracted access to all functions of the DM1X00. In addition to standard operating system functions, such as thread and memory management, KnOS integrates complete driver stacks for IEEE1394 and USB. KnOS supports FLASH-based persistent storage, clock management and an interactive terminal shell.

On top of KnOS, a comprehensive set of object-oriented software libraries is offered (SDK). This software framework supports typical interface functions, e.g. buttons, switches, rotaries, LEDs, control and transport protocols (including AV/C, UPnP, TCP/IP and HTTP), and USB host/device classes.

For a complete list of software modules and supported applications, please visit **www.archwave.net**.

Reference Board

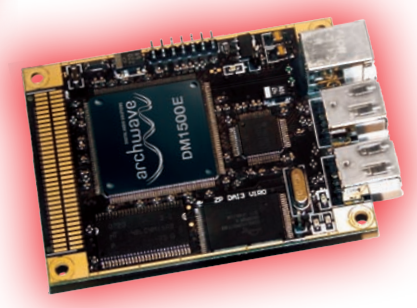


The DAI3 I/O Board is a full-fledged development board for audio breakout boxes, offering all types of audio and control interfaces and serving as the base board for the eBebob core modules. The board includes 8-channel analog I/O, electrical S/PDIF and optical ADAT or S/PDIF, MIDI I/O, UI elements including one rotary encoder, word clock sync I/O and a UART for debugging.

The main connector supports all the different eBebob core modules (DM1100E module for IEEE1394 applications, DM1500E module for IEEE1394 and USB2.0 applications).

The reference design includes the necessary power supplies and is also capable of accepting remote power from the IEEE1394 bus.

ZP Engineering DAI3 Module (1394+USB)



The DAI3 Module from ZP Engineering in conjunction with the eBebob I/O Board offers the full range of Bebob 5.x options, for both 1394- and USB2.0-based applications.

Ordering Info

Ordering Code	Description	
Bebob Package		
BCOIC-DM1100E-CQL	DM1100E Media Networking Processor (IEEE 1394 only)	
BCOIC-DM1100F-CQL	DM1100F Media Networking Processor (IEEE 1394 & USB 2.0)	
BCOIC-DM1500E-CQL	DM1500E Media Networking Processor (IEEE 1394 & USB 2.0)	
Bebob SDK + DDK		
BCOSDK-BOB-TDLA	Archwave enhanced Breakout Box SDK	
BCODDK-BOB-TDLA	Archwave IEEE1394/USB2.0 WDM/ASIO driver for Windows®	
Evaluation Hardware		
DAI1	DM1500E	ZP Engineering DAI1 Module (IEEE1394 only)
	DM1100E/F	ZP Engineering DAI1 Module (IEEE1394 only)
DAI3	DM1500E, DM1100F	ZP Engineering DAI3 Module (IEEE1394 and USB2.0)
A.eBebob_IO1-BRD-A1	eBebob I/O Board, Revision 1.0	
Evaluation Software		
Free downloads	• Precompiled Bebob applications for all reference designs • Archwave IEEE1394 and USB2.0 audio drivers for all reference designs • Executables for Windows® and Mac OS X mixer panels	
Free downloads (requires signed TDLA)	• Source code for Windows® and Mac OS X mixer panels	

Contact Info

Please visit **www.archwave.net** for further information.
For information on DAI3 Module and their pricing and order enquiries, please contact ZP Engineering srl: **www.zpeng.com**.

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